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QUESTION BANK (DESCRIPTIVE)

Subject with Code : Digital Logic Design(19CS0503) **Course & Branch**: B.Tech - CSE

Year &Sem: I-B.Tech& II-Sem

UNIT –I

Binary Systems&Boolean Alegebra

1. a) Convert the following numbers (L5) (6M)
   i)$(41.6875)_{10}$ to Hexadecimal number ii)$(11001101.0101)_2$ to base-8 and base-4
   iii)$(4567)_{10}$ to base2
   b) Subtract $(111001)_2$ from (101011) using 2's complement? (L5) (6M)

2. Prove the following identities:
   (i) A' B' C' + A' B C' + A B' C' + A B C' = C'. (L5)(6M)
   (ii) A B + A B C + A' B + A B' C = B + A C. (L5)(6M)

3. a)Convert the following numbers (L5) (3M)
   i) $(AB)_{16}$ = ( )$_2$ ii)) $(1234)_8$ = ( )$_{16}$ iii)$(101110.01)_2$=( )$_8$
   b) Convert the following to binary and then to gray code $(AB33)_{16}$ (L5) (4M)
   c) Perform the following Using BCD arithmetic $(7129)_{10}$ + $(7711)_{10}$ (L5) (5M)

4 Reduce the following Boolean Expressions to the indicated number of literals:
   (a) A'C'+ABC+AC'+AB' to two literals. (L6)(4M)
   (b) (X'Y'+Z')+Z+XY+WZ to three literals. (L6)(4M)
   (c) A'B(D'+CD)+B(A+A'CD) to one literal. (L6)(4M)

5. Explain the Binary codes with examples? (L2) (10M)
6 Explain about complements with examples? (L2) (10M)
7 a)Simplify the Boolean expressions to minimum number of literals (L6) (6M)
   i) X' + XY + X Z' + XYZ' ii) (X+Y) (X+Y')
   b) Obtain the Complement & Dual of Boolean Expression (L5) (6M)
   i) A+B+A'B'C ii) AB + A (B +C) + B'(B+D)
8 Convert the following (L6) (12M)

   a)$(1AD)_{16}$=( )$_{10}$ b) $(453)_8$=( )$_{10}$ c) $(10110011)_2$=( )$_{10}$ d) $(5436)_{10}$=( )$_{16}$

9 a) Convert the given expression in standard POS form: Y = (A + B) (B + C) (A + C). (L6) (6M)

b)Convert the following numbers (L6) (6M)

i) $(615)_{10}$ = ( )$_{16}$ ii)) $(214)_{10}$ = ( )$_{8}$ iii)$(0.8125)_{10}$=( )$_{2}$
iv) $(658.825)_{10}$=( )$_{8}$ v)$(54)_{10}$=( )$_{2}$

10 a) Express the Boolean function F=A+B'C as a sum of minterms. (L1) (6M)
b) Convert the given expression in standard POS form:Y=A(A+B+C) (L6) (6M)

UNIT –II

Gate Level Minimization

1. Simplify the following Boolean expression using K-MAP and implement using NAND gates. F(W,X,Y,Z) = XYZ+WXY+WYZ+WXZ (L6) (12M)
2. Simplify the Boolean expression using K-MAP F(A,B,C,D) =∑m(1,2,3,8,9,10,11,14) +d(7,15) (L6) (12M)
3. Simplify the Boolean expression using K-map and implement using NAND gates
   F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14) (L6) (12M)
4. Reduce the expression f(x,y,z,w)= πM(0,2,7,8,9,10,11,15) .d (3,4) using K-Map? (L6) (12M)
5. Simplify the Boolean expression using K-map? (L6)(12M)
   F(A,B,C,D,E)= ∑m(0,1,4,5,16,17,21,25,29)
6. Obtain the minimal product of sums and design using NAND gates (L1)(12M)
   F(A,B,C,D)= = ∑m(0,2,3,6,7) +d(8,10,11,15)
7. Explain NAND- NOR implementations? (L2) (12M)
8. a) Design the circuit by Using NAND gates F= ABC'+ DE+ AB'D' (L6) (6M)
   b) Design the circuit by Using NOR gates F= (X+Y). (X'+Y'+Z') (L6) (6M)
9. Simplify the Boolean expression using K-MAP (L6) (12M)
   F(A,B,C,D,E)= ∑m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)
10. Simplify the Boolean expression using K-MAP (L6) (12M)
    F(A,B,C,D) = πM (3,5,6,7,11,13,14,15) .d(9,10,12)

UNIT –III

Combinational Logic

1. Draw and explain the working of a Carry- Look ahead adder? (L2) (12M)
2. A)Implement the following Boolean function using 8:1 multiplexer (L5) (6M)

   $F(A, B, C, D) = A'BD' + ACD + A'C' D + B'CD$

   B) Explain about parallel adder? (L2)(6M)
3. A) Explain Design Procedure of combinational circuits? (L2) (6M)

   B) Explain Full binary subtractor in detail? (L2) (6M)
4. Design the combinational circuit binary to gray code? (L5) (12M)
5. A)Explain about Binary Half Adder? (L2) (6M)

   B)Design and draw a full adder circuit. (L5) (6M)
6. A)Implement the following Boolean function using 8:1 multiplexer (L5)(6M)

   $F(A,B,C.D) = \Sigma M(0,1,2,5,7,8,9,14,15)$

   B) Explain about Decimal Adder? (L2) (6M)
7. A)Design a 4 bit adder-subtractor circuit and explain the operation in detail? (L5) (6M)

   B) Explain the functionality of a Multiplexer? (L2) (6M)
8. Implement BCD to 7-segment decoder for common anode using 4:16 decoder? (L5) (12M)
9. A)Design a 4 bit binary parallel subtractor and the explain operation in detail? (L5) (6M)

   B) Design the combinational circuit of Binary to Excess-3 code convertor? (L5) (6M)
10. A) What is combinational circuits and explain analysis and design procedure of combinational circuits (L1)(6M)

    B) Explain about Priority encoder? (L2) (6M)

UNIT –IV

Synchronous Sequential Logic

1. A) Explain the Logic diagram of JK flip-flop? (L2) (6M)

   B) Write difference between Combinational & Sequential circuits? (L5) (6M)
2. A) Explain the Logic diagram of SR flip-flop? (L2) (6M)

   B) Design and draw the 3 bit up-down synchronous counter? (L5) (6M)
3. A) Draw and explain the operation of D Flip-Flop? (L2) (6M)

   B) Explain about Shift Registers? (L2) (6M)
4. A) Draw and explain the operation of T Flip-Flop? (L5) (6M)

   B) Explain about Ring counter? (L2) (6M)
5. A) Explain about ripple counter? (L2) (6M)

B) What is state assignment? Explain with a suitable example? (L1) (6M)

6. Explain the working of the following (L2 & L5) (12M)

i) J-K flip-flop

ii) S- R flip-flop

iii) D flip-flop

7. Explain the design of a 4 bit binary counter with parallel load in detail? (L2) (12M)

8. What is race-around condition? How does it set eliminate is a Master –slave J-K flip-flop? (L1)(12M)

9. A) Explain synchronous and ripple counters compare their merits and demerits? (L2) (6M)

B) Design a 4 bit binary synchronous counters with D-flip flop? (L5) (6M)

10.a)Write the truth table of clocked T- Flip Flop? (L1)**(**4M**)**

b) Write the differences between latches and flip flops? (L1)(4M)

c) Write the differences between synchronous and asynchronous counters? (L1)(4M)

UNIT –V

Memory and Programmable Logic

1. Explain about Error correction & Detection Codes with examples? (L2) (12M)
2. A) Write short notes on PLA. (L5) (4M)
   B) Implement the following Boolean function using PLA: (L5) (8M)
   F1(A,B,C)=Σm(3,5,6,7)
   F2(A,B,C)=Σm(0,2,4,7)
3. Implement the following function using PLA (L5)(12M)
   A(x,y,z)=∑m(1,2,4,6) B(x,y,z)=∑m(0,1,6,7) C(x,y,z)=∑m(2,6)
4. Design a Combinational circuit using PAL by considering the following Boolean Functions given in sum of minterms: (L5)(12M)
   W(A,B,C,D)=ΣM(2,12,13)
   X(A,B,C,D)=Σm(7,8,9,10,11,12,13,14,15)
   Y(A,B,C,D)=Σ(0,2,3,4,5,6,7,8,10,11,15)
   Z(A,B,C,D)=Σ(1,2,8,12,13)
   (L5)(12M)
5. What is memory decoding? Explain about the construction of 4 X 4 RAM ? (L1 &L2) (12M)
6. Construct the PROM using the conversion from BCD code to Excess-3 code? (L3)(12M)
7. Implement the following functions using PLA. (L5)(12M)
   A(x,y,z) = ∑m(1,2,4,6) B(x,y,z) = ∑m(0,1,6,7) c(x,y,z) = ∑m(2,6)
8. Construct the PLA using the conversion from BCD code to Excess-3 code? (L3)(12M)
9. A) Write difference between PROM ,PLA &PAL? (L5) (6M)
   B) Implement the following Boolean expressions using ROM (L5)(6M)
   F1(A,B,C)=Σ(m(0,2,4,7)
   F2(A,B,C)=Σm(1,3,5,7)
10. A)What is ROM?List the different types of ROMs. (L1&L4) **(**6M)
    B)Implement following Boolean functions using PLA (L5) (6M)
    F1(A,B,C)=Σm(0,1,3,5) and F2(A,B,C)=Σm(0,3,5,7)